

1 CLAIMS:

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3 1. A semiconductor processing method of forming transistors  
4 comprising:

5 forming a plurality of shallow trench isolation regions received  
6 within a substrate, the shallow trench isolation regions being formed to  
7 define a plurality of active areas having widths within the substrate,  
8 some of the widths being no greater than about one micron, at least  
9 two of the widths being different; and

10 forming a gate line over respective active areas to provide  
11 individual transistors, the transistors corresponding to the active areas  
12 having the different widths having different threshold voltages.

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14 2. The semiconductor processing method of claim 1 further  
15 comprising for the transistors having the different widths, providing the  
16 different threshold voltages without using a separate channel implant for  
17 the transistors.

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19 3. The semiconductor processing method of claim 1, wherein the  
20 two different widths are each less than one micron.  
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1           4.     The semiconductor processing method of claim 1, wherein the  
2 different threshold voltages are each less than 2 volts.

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4           5.     The semiconductor processing method of claim 1, wherein the  
5 different threshold voltages are each less than 1 volt.

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7           6.     The semiconductor processing method of claim 1, wherein the  
8 two different widths are each less than one micron, and the different  
9 threshold voltages are each less than 2 volts.

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11           7.     The semiconductor processing method of claim 1, wherein the  
12 two different widths are each less than one micron, and the different  
13 threshold voltages are each less than 1 volt.  
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2 8. A method of forming a pair of field effect transistors comprising:

3 forming a pair of active areas over a substrate, one of the active  
4 areas having a width less than one micron;

5 forming a gate line over both active areas to provide a pair of  
6 transistors having different threshold voltages, the transistors being  
7 provided with the different threshold voltages without using a separate  
8 channel implant for either transistor; and

9 wherein the transistor with the lower of the threshold voltages  
10 corresponds to the active area having the width less than one micron.

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12 9. The method of claim 8 further comprising forming the  
13 transistor having the higher of the threshold voltages to have an active  
14 area width greater than one micron.

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16 10. The method of claim 8 further comprising forming the  
17 transistor having the higher of the threshold voltages to have an active  
18 area width less than one micron.

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20 11. The method of claim 8 further comprising conducting only  
21 one common channel implant for the pair of transistors.

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1 12. The method of claim 8, wherein the forming of the pair of  
2 active areas comprises forming shallow trench isolation regions received  
3 within the substrate proximate the active areas.  
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5 13. The method of claim 8, wherein the forming of the gate line  
6 comprises forming a common gate line over the active areas.  
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8 14. The method of claim 8, wherein the forming of the gate line  
9 comprises forming a common gate line over the active areas, the  
10 transistors being formed in a parallel configuration.  
11

12 15. A method of forming integrated circuitry comprising  
13 fabricating two field effect transistors having different threshold voltages  
14 without using a separate channel implant for one of the transistors  
15 versus the other.  
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17 16. The method of claim 15, wherein the fabricating of the two  
18 field effect transistors comprises forming at least one active area of one  
19 of the transistors to have a width less than one micron.  
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17. The method of claim 15, wherein the fabricating of the two field effect transistors comprises forming both active areas of the transistors to have widths less than one micron.

18. The method of claim 15, wherein the fabricating of the two field effect transistors comprises forming both active areas of the transistors to have different widths.

19. The method of claim 15, wherein the fabricating of the two field effect transistors comprises forming both active areas of the transistors to have different widths, each of which being less than one micron.

20. The method of claim 15, wherein the fabricating of the two field effect transistors comprises forming shallow trench isolation regions within a substrate proximate the two field effect transistors, the shallow trench isolation regions defining, at least in part, active area widths of the transistors.

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1 21. A semiconductor processing method comprising forming two  
2 series of field effect transistors over a substrate, one series being  
3 isolated from adjacent devices by shallow trench isolation, the other  
4 series having active area widths greater than one micron, the one series  
5 being formed to have active area widths less than one micron to achieve  
6 lower threshold voltages than the other of the series.

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8 22. The semiconductor processing method of claim 21, wherein  
9 the threshold voltages for the two series of field effect transistors are  
10 defined by a common channel implant.

11  
12 23. The semiconductor processing method of claim 21, wherein  
13 the threshold voltages for the two series of field effect transistors are  
14 defined by a common channel implant, said implant being the only  
15 channel implant which defines the threshold voltages for the two series  
16 of field effect transistors.

17  
18 24. The semiconductor processing method of claim 21, wherein  
19 the threshold voltages for the two series of field effect transistors are  
20 defined by one or more common channel implants.

1 25. The semiconductor processing method of claim 21, wherein  
2 the threshold voltages for the two series of field effect transistors are  
3 defined by one or more common channel implants, said common channel  
4 implants being the only channel implants which define the threshold  
5 voltages for the two series of field effect transistors.

6  
7 26. A semiconductor processing method comprising forming two  
8 series of field effect transistors over a substrate, at least one series  
9 being isolated from adjacent devices by shallow trench isolation, and  
10 further comprising achieving different threshold voltages between field  
11 effect transistors in different series by varying the active area widths of  
12 the field effect transistors in the series, at least one series having active  
13 area widths less than one micron.

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15 27. The semiconductor processing method of claim 26, wherein  
16 the threshold voltages for the two series of field effect transistors are  
17 defined by a common channel implant.  
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1           28. The semiconductor processing method of claim 26, wherein  
2 the threshold voltages for the two series of field effect transistors are  
3 defined by a common channel implant, said implant being the only  
4 channel implant which defines the threshold voltages for the two series  
5 of field effect transistors.

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7           29. The semiconductor processing method of claim 26, wherein  
8 the threshold voltages for the two series of field effect transistors are  
9 defined by one or more common channel implants.

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11           30. The semiconductor processing method of claim 26, wherein  
12 the threshold voltages for the two series of field effect transistors are  
13 defined by one or more common channel implants, said common channel  
14 implants being the only channel implants which define the threshold  
15 voltages for the two series of field effect transistors.



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1 31. A semiconductor processing method of forming dynamic  
2 random access memory circuitry comprising:

3 providing a substrate having a memory array area over which  
4 memory circuitry is to be formed, and a peripheral area over which  
5 peripheral circuitry is to be formed;

6 forming a plurality of shallow trench isolation regions received  
7 within the peripheral area of the substrate, the shallow trench isolation  
8 regions being formed to define a plurality of active areas having widths  
9 within the substrate, some of the widths being no greater than about  
10 one micron, at least two of the widths being different; and

11 forming a conductive line over respective active areas to provide  
12 individual transistor gates, the transistors corresponding to the active  
13 areas having the different widths having different threshold voltages.

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15 32. The semiconductor processing method of claim 31 further  
16 comprising for the transistors having the different widths, providing the  
17 different threshold voltages without using a separate channel implant for  
18 the transistors.

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20 33. The semiconductor processing method of claim 31, wherein  
21 the two different widths are each less than one micron.  
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34. A transistor assembly comprising:

a plurality of active areas having widths defined by shallow trench isolation regions of no greater than about one micron, at least some of the widths being different; and

gate lines disposed over the plurality of active areas to provide individual transistors, those transistors whose widths are different having different threshold voltages from one another.

35. The transistor assembly of claim 34, wherein the threshold voltages of at least some of the individual transistors are less than one volt.

36. The transistor assembly of claim 34, wherein individual transistors having active areas with the smaller widths have threshold voltages which are smaller than other individual transistors having active areas with larger widths.

37. The transistor assembly of claim 34, wherein one of the transistors comprises a portion of precharge circuitry for dynamic random access memory circuitry.

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1 38. The transistor assembly of claim 34, wherein one of the  
2 transistors comprises a pass transistor.

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4 39. The transistor assembly of claim 34, wherein one of the  
5 transistors comprises a portion of sense amplifier circuitry for dynamic  
6 random access memory circuitry and has a lower threshold voltage  $V_{th}$ .

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8 40. The transistor assembly of claim 34, wherein some of the  
9 transistors are joined together in a parallel configuration.

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11 41. Dynamic random access memory circuitry comprising:  
12 a substrate having a memory array area for supporting memory  
13 circuitry and a peripheral area for supporting peripheral circuitry;  
14 a plurality of active areas within the peripheral area having widths  
15 defined by shallow trench isolation regions of no greater than about one  
16 micron, at least some of the widths being different; and  
17 conductive lines disposed over the plurality of active areas to  
18 provide individual transistors, those transistors whose widths are different  
19 having different threshold voltages from one another.  
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1 42. The dynamic random access memory circuitry of claim 41,  
2 wherein the threshold voltages of at least some of the individual  
3 transistors are less than one volt.  
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5 43. The dynamic random access memory circuitry of claim 41,  
6 wherein individual transistors having active areas with the smaller widths  
7 have threshold voltages which are smaller than other individual transistors  
8 having active areas with larger widths.  
9

10 44. A transistor assembly comprising:  
11 an active area;  
12 a plurality of spaced-apart shallow trench isolation regions received  
13 by the active area and defining active sub-areas therebetween, individual  
14 active sub-areas having respective widths, at least one of the widths  
15 being no greater than about one micron and at least one other sub-area  
16 having a width which is different from the one width; and  
17 a gate line extending over the one and the other sub-area and  
18 defining, in part, separate transistors, wherein the separate transistors  
19 have different threshold voltages.  
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45. The transistor assembly of claim 44, further comprising a gate line extending over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron.

46. The transistor assembly of claim 44, further comprising a gate line extending over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron, wherein more than two of the plurality of transistors have different threshold voltages.

47. The transistor assembly of claim 44, wherein said gate line comprises a common gate line which extends over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron.

48. The transistor assembly of claim 44, wherein said gate line comprises a common gate line which extends over a plurality of the active sub-areas defining a plurality of transistors, each active sub-area width of an associated transistor being no greater than about one micron and said plurality of transistors being joined in a parallel configuration.

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1 49. A transistor assembly comprising:

2 an active area;

3 a plurality of spaced-apart shallow trench isolation regions received  
4 by the active area and defining active sub-areas therebetween, individual  
5 active sub-areas having respective widths, at least one of the widths  
6 being no greater than about one micron and at least one other sub-area  
7 having a width which is less than the one width; and

8 a gate line extending over the one and the other sub-area and  
9 defining, in part, separate transistors, wherein the separate transistors  
10 have different threshold voltages, wherein said gate line comprises a  
11 common gate line which extends over a plurality of the active sub-areas  
12 defining a plurality of transistors, each active sub-area width of an  
13 associated transistor being no greater than about one micron and said  
14 plurality of transistors being joined in a parallel configuration to provide  
15 a pull down circuit coupled to a common node.

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17 50. The transistor assembly of claim 49, further comprising a  
18 sense amplifier formed from pair of transistors, each of the pair having  
19 a gate that is cross-coupled to a drain of another of the pair, sources  
20 of the pair being coupled to the common node.  
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